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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
IVT.0032US

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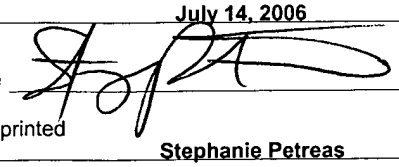
on July 14, 2006

Signature 

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Application Number	Filed
10/690,263	October 21, 2003

First Named Inventor	
Dominik J. Schmidt	
Art Unit	**Examiner**
2181	Richard B. Franklin

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 42,117
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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512-418-9944
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July 14, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [x] *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Dominik J. Schmidt	§	Group Art Unit:	2181
		§		
Serial No.:	10/690,263	§		
		§	Examiner:	Richard B. Franklin
Filed:	October 21, 2003	§		
		§		
For:	Integrated Circuit Capable Of Working With Multiple Bus Interface Standards	§	Atty. Dkt. No.:	IVT.0032US
		§		
		§		

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Commissioner for Patents
P.O. Box 1450
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REASONS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

Applicant seeks pre-appeal review of the rejection of claims 1, 2 and 4-6 under 35 U.S.C. §102(b), and the rejection of claims 3 and 7-10 under 35 U.S.C. §103(a). It is respectfully submitted that these rejections are clearly erroneous, and the burden of an appeal should be avoided.

Pending claims 1, 2 and 4-6 stand rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,793,989 (Moss). As to claim 1, Moss nowhere teaches: (1) a common set of pins coupled to first and second interface circuits and a host computer bus; (2) such common set of pins communicating with the host computer bus in accordance with either a first or second bus standard; or (3) the common set of pins being user selectable.

As to point (1), the Examiner contends that the common set of pins is taught by Moss as element 105, which Moss teaches is a female mechanical connector. However, this connector is not coupled to both multiple interface circuits and a host computer bus. Instead, Moss teaches that the connector 105 is connected to a card logic unit 111 and a corresponding mechanical connector 107 of an applications device 103. As such, the peripheral device 101 of which connector 105 is a part is not coupled to a host computer bus. Instead, it is simply coupled to the

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Stephanie Petreas

applications device 103. Accordingly, Moss fails to teach a common set of pins coupled to both of multiple interface circuits and a host computer bus.

Furthermore, nowhere does Moss teach that such (non-existent) common pins communicate with the host computer bus in accordance with either of the first or second bus standards. In fact, Moss teaches the opposite. That is, in Moss only RS-232 signals are communicated with I/O bus 127 (contended by the Examiner to be the computer bus). Because claim 1 recites that communication with a host computer bus is to be in accordance with either of two bus standards, the permanent RS-232 connection to I/O bus 127 taught in Moss cannot meet the claimed subject matter.

The Examiner further contends that the common set of pins of Moss is user selectable "because the user ultimately in the end selects the pin format." Final Office Action, p. 3. It is unclear what the Examiner is referring to in this regard, as there is no support in Moss for such "ultimate user selection." That is, in Moss there is no mention of a user, nor that the user makes a selection of a bus standard with which common pins communicate with a host computer bus. Furthermore, the Examiner appears to concede that it is not a user that makes the selection: instead, the Examiner contends that it is socket logic unit 109 of the applications device 103 that "represents the 'user selectable' function...." Final Office Action, p. 3. However, all that Moss teaches with regard to socket logic 109 is that a unique code can be set or presented. However, nowhere does Moss teach that such code be user set. Furthermore, no matter how socket logic unit 109 is set, communication with the host computer bus is still only with regard to a single bus standard. That is, as described above, there is no communication with a host computer bus in Moss in accordance with multiple bus standards. Accordingly, the rejection of claim 1 and the claims depending therefrom is clearly erroneous.

The rejection of dependent claim 5 is further clearly erroneous, as Moss nowhere teaches a multi-voltage I/O buffer coupled to each pin. Instead, the Examiner merely refers to tri-state buffers that act as multiplexing switches within card logic unit 111. Such multiplexing switches are not multi-voltage I/O buffers. As to dependent claim 6, Moss nowhere teaches an internal bus coupled to *both* first and second interface circuits. In this regard, the Office Action refers to items 114, 115, 116 and 119 of Moss. However, as clearly taught and shown in Moss each of these buses are independent buses and no one of these buses couples to both interface circuits.

Moss, FIG. 1. Accordingly, Moss fails to teach a single internal bus that is coupled to multiple interface circuits. For this further reason, the rejection of claim 6 is clearly erroneous.

For at least the same reasons as claim 1, the rejection of dependent claim 3 under §103(a) over Moss in view of Tyson "How PCI Works" is similarly improper. Furthermore, while Tyson teaches that computers use a PCI bus to connect peripherals, there is no suggestion or motivation to combine such a bus with the peripheral device of Moss. In this regard, "the mere fact that references can be combined or modified does not render the resulting combination obvious unless the prior art also suggest the desirability of the combination." *In re Mills,* 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). As such, the rejection of claim 3 is clearly erroneous as neither reference provides any rationale suggesting the desirability of the combination. MPEP §2143.01.

As to dependent claims 7 and 8, which stand rejected under 35 U.S.C. §103(a) over Moss alone, this rejection is clearly erroneous at least for the same reasons discussed above regarding claims 1 and 6. The rejection is further erroneous, as there is no teaching or suggestion in Moss for an interface circuit that formats signals on an internal bus that is coupled to both interface circuits. Instead, as described above in Moss, dedicated buses exist, namely dedicated buses 114 and 116 and dedicated buses 115 and 119, each of which provides signals of only a single bus standard to the interface circuits.

For at least the same reasons described above as to claim 1, the rejection of claims 9 and 10 under §103(a) over Moss in view of U.S. Patent No. 6,871,244 (Cahill) is similarly erroneous. Further with regard to claim 10, neither Moss nor Cahill anywhere teaches or suggests the presence of multiple power supplies to supply voltage swings in accordance with multiple bus standards. Instead, Cahill merely teaches a single power supply that provides an output voltage that may be converted to different voltages. However, Cahill nowhere teaches or suggests the presence of multiple power supplies. Of course, Moss teaches nothing in this regard. For this further reason, the rejection of dependent claim 10 is clearly erroneous.

Because the above rejections are clearly erroneous, the need for an appeal should be avoided.

Respectfully submitted,

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